## REMARKS

The above Amendments and these Remarks are in reply to the Office Action mailed May 11, 2005.

Currently, claims 1-36 are pending. Applicants respectfully request reconsideration of claims 1-36

I. Summary of the Examiner's Objections

Claims 1-3, 5-17, 19, 20 and 25-36 were rejected under 35 USC 102(b) as being anticipated by *Etoh et al.* (USP RE37593).

Claims 4 and 18 were rejected under 35 USC 103(a) as being unpatentable over *Etoh et al.* (USP RE37593) in view of *Hellums* (5,362,988) (previously cited).

Claims 21-24 were rejected under 35 U.S.C. 103(a) as being unpatentable over *Etoh et al.* (USP RE37593).

II. Summary of the Amendments

Claims 1, 2, 16, 25 and 32 have been amended.

III. Remarks

The Examiner is thanked for the brief remarks in the Advisory Action issued in reply to Applicant's Response after Final Action (Response B) indicating a brief response to applicants remarks in the claims.

It is respectfully submitted claims 1-3, 5-17, 19, 20 and 25-36 are not anticipated by *Etoth et al.* because:

- *Etoh* does not teach a host device which provides both host voltage and a power up complete signal.
- The alleged bypass enable signal (LM) is not responsive to a signal generated by the host device indicating that power up is complete. LM is responsive to the "host voltage" and the "host voltage" does not indicate power up of the circuit of *Etoh* is complete.
- *Etoh* does not show "a controller" that the bypass signal is operable by the controller. This limitation has been present in some form in claims 5, 31, and 34, but the Examiner

has never identified a component of *Etoh et al.* disclosing this element of the claimed invention.

**Claim 1-3, 4 – 15**

Claim 1 calls for:

1. A memory system including a control path to a host device, the host device supplying ***a host voltage and a power up complete signal***, comprising:

...;

a controller;

...

a bypass enable signal ***operable by the controller*** responsive to the power up complete signal generated by the host device ***indicating that the power up of the host is complete***.

Initially, it is noted that the "host voltage" and the "signal generated by the host device indicating that the power up of the host is complete" are separate elements of the claim. In order to anticipate claim 1 of the present application, the *Etoh* patent must disclose both "a host voltage" and a "power up complete signal" arranged in the manner set forth in the claims of the present application.

"A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). (MPEP §2131). Hence, all of the elements called for in the present claims must be shown to be anticipated.

The Examiner states in the Advisory action:

As shown in *Etoh et al.*'s figure 1A, signal LM is responsive to signal Vcc, and signal Vcc is responsive to signal 4. Therefore, signal LM is responsive to signal 4.

Neither signal 4 nor the LM signal comprises a "power up complete signal generated by the host device indicating that the power of lof the host is complete"

Signal 4 operates switch SW in a case where external power is lost:

Numeral 2 is an exemplary power supply circuit which detects a drop of an external

> power supply voltage (Vext) to shift the LSI chip into a back-up state by a battery. This power supply circuit serves to prevent data stored in the LSI chip from disappearing even when Vext is lowered due to shut-down of the commercially available power source. ...numeral 3 is a voltage drop detection circuit for the power supply voltage, SW is a switch for preventing current from flowing the battery to an external power supply terminal during data retention, numeral 4 is a control signal for the switch, B is a battery by which the entire LSI chip operates in the data retention mode (Vbt is its voltage)...

Hence, signal does not indicate that power up of the host is complete, but that external power is missing. Signal 4 is responsive to the voltage drop circuit, which is responsive to the "power supply voltage".

LM is also responsive to the external voltage:.:

> Numeral 10 is a circuit for generating a limiter enable signal LM. If the external power supply voltage is higher than the internal power supply voltage, thereby operating the voltage converter circuit (voltage limiter), LM of a high voltage ("1") is generated whereas if the external power supply voltage is decreased to a value equal to the internal power supply voltage, LM of a low voltage of ("0") is generated. In the latter case, the external power supply voltage is directly applied to the main circuit block and also the voltage converter is not operated to restrain power consumption. In the example as shown, when the power supply voltage Vcc is compared with the reference voltage Vcx, and LM is generated if the former is larger than the latter. (Col 6, lines 23 – 36)

There is no explicit indication in the specification of what happens to LM when the circuit is in "data retention" mode (e.g. when signal 4 operates switch SW). Moreover, the specification specifically states that signal LM is responsive to the external voltage, ***not*** signal 4 – Signal 4 itself is generated in response to the external voltage.

As such, there is no "... bypass enable signal operable *responsive to a signal generated by the host device indicating that the power up of the host is complete"*. The external supply voltage cannot anticipate both elements of claim 1, and there is no signal which provides an indicator that "*the power up of the host is complete"*.

In addition, there is no "controller" included in a memory system disclosed in *Etoh et al.*, nor one which provides a "a bypass enable signal *operable by the controller"*.

The above amendment is supported in the specification as follows:

> Upon application of a BYPASS signal, under the direction of the controller 160, the bypass transistor shorts the input voltage between VDD and the output. ...

the controller waits for a indicator signal from the host device that power up has been completed. In one embodiment, the threshold voltage is 2.4 volts, distinguishing between 1.8 volt +/- 10% operation or 3.0 volt +/- 10% operation. In a further embodiment, where the device is an MMC card, this signal may be CMD0 or CMD1, the initial two commands sent by a host to an MMC card which are generally used to reset all cards to idle state and request and confirm operating conditions. In other technologies, any initial signal indicating the completion of power up of the host device, specifically designed for that purpose or indicating completion by its nature may be used as the indicator signal.

As such, at least two elements defined in claim 1 are not disclosed in *Etoh et al.*

Therefore, it is respectfully submitted claims 1, and claims 2-3, 5-15 dependent from claim 1 and including all the limitations thereof, are not anticipated by *Etoh et al.*

**Claims 16 – 17, 19, 20**

For substantially the same reasons as set forth above, it is respectfully submitted claims 16 – 17, 19, 20 are not anticipated by *Etoh et al.*

Claim 16 includes limitations calling for:

A method for operating a voltage regulator in a memory system including a controller, comprising:

providing ...a regulator bypass responsive to the controller shorting the host voltage at the input to the output responsive to an enable signal;

...

responsive to a power up completion signal from a host device to the controller, determining the power supplied by the host; and

if the power is below a threshold operating voltage, enabling the bypass using the controller.

As noted with respect to claim 1, the elements of *Etoh et al.* do not provide a "power up completion" signal, but merely a an external voltage to a memory device. There is no separate signal for power up completion of a host.

Moreover, there is no teaching of " ... setting the bypass to off prior to power up of a host device..." In the rejection, the Examiner cites no support for this element. Examination of the reference yields no disclosure of an equivalent step in combination with the other steps of this claim.

...

a voltage regulator having a shorting element between a host voltage input and an output, the shorting element being responsive to a bypass control signal, *the bypass control signal provided by the controller responsive to a host system power up complete signal* which enables the shorting element when the host supply voltage provided by the host is below a threshold level.

No separate "controller" is taught in *Etoh et al.*, nor is a "...the bypass control signal provided by the controller responsive to a host system power up complete signal". In the instant claim, the limitation is specific as to the origin of the bypass control signal as "provided by the controller" Since no "controller" is disclosed in *Etoh et al.*, no such signal can be provided.

Hence, it is respectfully submitted claim 34 and claims 35 - 36 dependent from claim 34 are not anticipated by *Etoh et al.*

**Claim 4 and 18**

Claims 4 and 18 were rejected as obvious over *Etoh et al.* in view of *Hellums* (U. S. Patent No 5,362, 988.) As understood, *Hellums* is cited for the proposition that the bypass can comprise a plurality of transistors. (The Examiner's reference to "transistor TOS" is not understood – no such transistor can be found in either reference. It is understood that the examiner is referring to the bypass, previously alleged to be SWa of *Etoh et al.)*

Claims 4 and 18 depend from claims 1 and 16 respectfully, and it is respectfully submitted one of average skill in the art would not be led by the teachings of Claims 4 and 18 to provide an apparatus or method wherein a bypass is enabled responsive to "...a signal generated by the host device indicating that the power up of the host is complete." In *Etoh et al.,* the control path is understood to be provided by the IO buffer:

> Numeral 7 is an input/output buffer circuit; numeral 11 is an input/output bus for transmitting/receiving control signals and data between ... The input/output buffer circuit 7, which also serves as a voltage level converting circuit, can transmit/receive the control signals and data even if the logic swing in the chip does not coincide with that in the outside

One of average skill would be required to modify the teachings of *Etoh et al.* to utilize a control signal from an external device via the IO buffer (7) to provide "... a signal generated by the host

Hence, two separate steps of claim 16 are wholly not disclosed in the reference.

It is therefore respectfully submitted claim 16, and claims 17, 19 - 20 dependent from claim 16 and including all the limitations thereof, are not anticipated by *Etoh et al.*.

**Claims 25 - 36**

For substantially the same reasons as set forth above, it is respectfully submitted claims 25 – 31 or 32 – 26 are not anticipated by *Etoh et al.*

Claim 25 includes limitations similar to those set for the above with respect to claim 1 and calls for:

> A peripheral device for a host system supplying a host voltage, the peripheral device including a voltage regulator circuit ***and a controller***, comprising:
>
> . . .
>
> a bypass control signal ***output from the controller*** coupled to the bypass element and responsive to a host system ***power up completed signal*** which enables the bypass element when the host voltage is below a threshold level.

No such host system power up completed signal enabling a bypass element is disclosed. No such bypass control signal output from the controller is disclosed. Hence, it is respectfully submitted claim 25 and claims 26 – 31 dependent there from are not anticipated by *Etoh et al.*

Claim 32 includes limitations similar to those set for the above with respect to claim 16 and calls for:

> setting the bypass to off prior to power up of a host device;
> responsive to a command signal from the host device, determining the power supplied by the host; and

No such command signal is from a host device nor controller is disclosed in *Etoh et al.* , nor is any step of "setting the bypass to off prior to power up" are provided . Hence, it is respectfully submitted claim 25 and claim 33 dependent from claim 32 are not anticipated by *Etoh et al.*

Claims 34 includes limitations similar to those set for the above with respect to claim 1 and calls for:

> a controller;

device indicating that the power up of the host is complete..." There are no teachings in *Etoh et al.* that such a control signal is required or desirable, nor to use the control signal to enable a bypass. Hence, three independent inventive changes are required in *Etoh et al.* in order to reach the invention of claim 4 or 18.

Thus, it is respectfully submitted claims 4 and 18 are not obvious.

**Claims 21 – 24**

Claims 21 - 24 were rejected as obvious over *Etoh et al.* However, it is respectfully submitted that claims 21 – 24 are not obvious over *Etoh et al.*

Claims 21 – 24 depend from claim 16. Claim 16 requires

> setting the bypass to off prior to power up of a host device;
> responsive to a power up completion signal from a host device to the controller, determining the power supplied by the host; and

One of average skill would be required to modify the teachings of *Etoh et al.* to utilize a control signal from an external device via the IO buffer (7) to provide "... a power up completion signal from a host device ..." and be required to set the bypass off. There are no teachings in *Etoh et al.* that such a control signal is required or desirable, nor to use the control signal to enable a bypass, nor anything as to the state of the bypasses (SWa) during power up. Hence, three independent inventive changes are required in *Etoh et al.* in order to reach the invention of claim 21 - 24.

Thus, it is respectfully submitted claims 21 - 24 are not obvious.

Based on the above amendments and these remarks, reconsideration of claims 1 - 36 is respectfully requested.

The Examiner's prompt attention to this matter is greatly appreciated. Should further questions remain, the Examiner is invited to contact the undersigned attorney by telephone.

Enclosed is a PETITION FOR EXTENSION OF TIME UNDER 37 C.F.R. § 1.136 for extending the time to respond up to and including today, November 14, 2005.

The Commissioner is authorized to charge any underpayment or credit any overpayment to Deposit Account No. 501826 for any matter in connection with this response, including any fee for extension of time, which may be required.

Respectfully submitted,

Date: November 14, 2005

By: _____

Larry E. Vierra
Reg. No. 33,809

VIERRA MAGEN MARCUS HARMON & DENIRO LLP
685 Market Street, Suite 540
San Francisco, California 94105-4206
Telephone: (415) 369-9660
Facsimile: (415) 369-9665